Highlights from the Nanoelectronics for 2020 and Beyond (*Nanoelectronics*) NSI

April 2017

The semiconductor industry will continue to be a significant driver in the modern global economy as society becomes increasingly dependent on mobile devices, the Internet of Things (IoT) emerges, massive quantities of data generated need to be stored and analyzed, and high-performance computing develops to support vital national interests in science, medicine, engineering, technology, and industry. These applications will be enabled, in part, with ever-increasing miniaturization of semiconductor-based information processing and memory devices. Continuing to shrink device dimensions is important in order to further improve chip and system performance and reduce manufacturing cost per bit. As the physical length scales of devices approach atomic dimensions, continued miniaturization is limited by the fundamental physics of current approaches. Innovation in nanoelectronics will carry complementary metal-oxide semiconductor (CMOS) technology to its physical limits and provide new methods and architectures to store and manipulate information into the future.

The Nanoelectronics Nanotechnology Signature Initiative (NSI) was launched in July 2010 to accelerate the discovery and use of novel nanoscale fabrication processes and innovative concepts to produce revolutionary materials, devices, systems, and architectures to advance the field of nanoelectronics. The Nanoelectronics NSI white paper[1] describes five thrust areas that focus the efforts of the six participating agencies[2] on cooperative, interdependent R&D:

1. Exploring new or alternative state variables for computing.
2. Merging nanophotonics with nanoelectronics.
3. Exploring carbon-based nanoelectronics.
4. Exploiting nanoscale processes and phenomena for quantum information science.
5. Expanding the national nanoelectronics research and manufacturing infrastructure network.

The following paragraphs provide examples of advancements that have been made toward the objectives of the Nanoelectronics NSI since its launch. Examples of relevant programs that have been created since the inception of the NSI to further advance these goals are also identified.

The exploration of alternative state variables for computing has enjoyed significant investment from numerous government agencies[2] as well private companies.[3] NSF investments have focused on upstream, exploratory research in new, alternative state variables for logic and memory components and on suitable computing architectures, computer-based research on new devices, integration of nanoelectronic and nanophotonic components into new systems, and new quantum information components and systems. Examples of core NSF activities that support this thrust are the Electronic and Photonic Materials program and the Electronics, Photonics, and Magnetic Devices program. Agencies under DOD support several projects that contribute to this signature initiative. The Defense Advanced Research Projects Agency (DARPA) is identifying promising approaches using nanotechnology to drive advances in new devices to replace transistors and to augment the performance of conventional transistor integrated circuits. DARPA's MesoDynamic Architectures program developed methods to modulate states and stabilize circuits

[1] www.nano.gov/NSINanoelectronics

[2] National Science Foundation (NSF), Department of Defense (DOD), National Aeronautics and Space Administration (NASA), National Institute of Standards and Technology (NIST), Department of Energy (DOE), and the Intelligence Community (IC).

[3] Raytheon, BBN Technologies, Hypres, Northrop Grumman, IBM, GLOBALFOUNDRIES, Intel Corporation, Micron Technology, and Texas Instruments

at quantum levels and has investigated new materials and device architectures that exploit intrinsic nonlinearities of mesoscale and nanoscale materials. Accomplishments have included the first-ever topological insulator thermoelectric device (Figure 1).[4] The Air Force Research Laboratory (AFRL) has targeted research programs to investigate potentially revolutionary advances in performance such as 2D electronic materials. For example, the Materials and Manufacturing Directorate at AFRL investigates nanoelectronic materials and their synthesis to improve device performance and reliability and to develop technologies that are less dependent on foreign foundries. NIST is making important advances in nanoelectronics by developing measurement methods to evaluate, and fabrication approaches to manufacture, high-performance materials and devices. In an effort to specifically address the measurement needs associated with this signature initiative, NIST formed the Nanoelectronics Group[5] to conduct basic research to advance the optical and electrical measurement science infrastructure necessary for innovation in future nanoelectronic and thin-film devices. A partnership between NIST, the Intelligence Advanced Research Projects Activity, and several private companies[6] will focus on the development of spin-based nanoscale cryogenic memory and logic for energy-efficient exascale computing, which is critical for many national priorities and for national security.[7] An additional partnership between NIST and DARPA on the Unconventional Processing of Signals for Intelligent Data Exploitation program seeks to exploit spin-based effects in nanostructures to develop non-Boolean computational methods for efficient pattern matching of complex signal inputs (e.g., video) in real time.

Public-private partnerships have played and will continue to play a critical role in the development of these promising technologies. Since 2005, the Nanoelectronics Research Initiative (NRI)[8] has supported long-range research toward the discovery of the fundamental building blocks for tomorrow's nanoscale electronics—new devices and circuit architectures for computing—that are viewed as essential to continuing advances in the performance of information technologies. Supported by a consortium of companies in the Semiconductor Industry Association, Federal agencies (NIST and NSF), and state and local governments, the NRI has sponsored 63 academic institutions involving 330 faculty members and 700 students, resulting in 3,362 publications and 62 patent applications.[9] In 2016, the Semiconductor Research Corporation (SRC) announced nanoelectronic COmputing REsearch (nCORE),[10] a $60 million+ public-private research program seeking to enable novel computing paradigms with improved efficiency, enhanced performance, and new functionalities. Since 2012, the DARPA-supported Semiconductor Technology Advanced Research Network (STARnet) program[11] has pursued an innovative approach to exploring nanoscale devices and new circuit architectures that

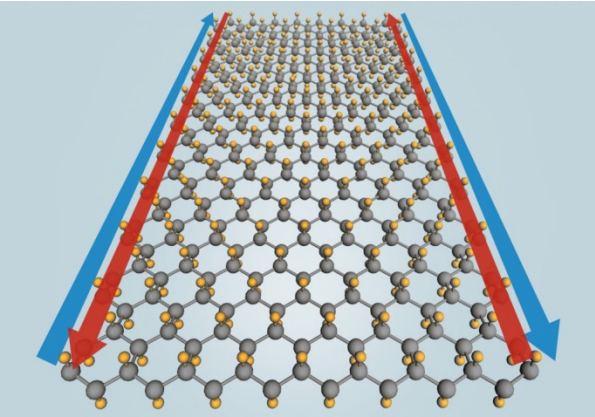

Figure 1. This image depicts the flow of electricity along the outside edges of a new topological insulator, stanene. (Source: DARPA)

[4] science.dodlive.mil/2013/12/26/the-new-state-of-quantum-matter-the-impact-on-electronics/
[5] www.nist.gov/pml/div683/grp04/index.cfm
[6] Raytheon, BBN Technologies, Hypres, Northrop Grumman, and IBM
[7] B. Baek, W. H. Rippard, S. P. Benz, S. E. Russek, P. D. Dresselhaus, Hybrid superconducting-magnetic memory device using competing order parameters. *Nature Communications* **5**, Article number 3888 (2014).
[8] www.src.org/program/nri/
[9] As of March 29, 2017
[10] www.src.org/compete/ncore/
[11] www.darpa.mil/program/starnet

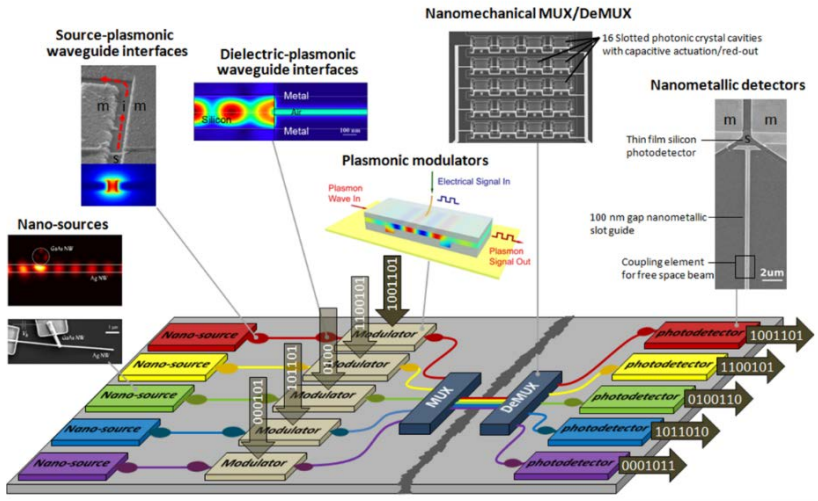

Figure 2. Concept for future high-performance hybrid nanophotonic chips. (Source: Stanford University)

could bring new functional capabilities and reduced power consumption. Funded as a public-private partnership by DARPA and U.S. semiconductor and supplier industries,[12] the STARnet program has helped maintain U.S. leadership in semiconductor technology. In 2016, the SRC announced the Joint University Microelectronics Program (JUMP), a new $150 million+ research program that will support long-term research focused on high-performance, energy-efficient microelectronics at participating universities. Both JUMP and nCORE will participate in the $6 million NSF Energy-Efficient Computing: from Devices to Architectures (E2CDA) program.

The merger of nanoelectronics and nanophotonics aims to exploit the potential of photonics to revolutionize the microelectronics industry. Based on current trends, multicore processors will have 1,000 cores or more within the next decade. However, their promise of increased performance will only be realized if their inherent scaling and programming challenges can be overcome. Fortunately, recent advances in nanophotonic device manufacturing are making CMOS-integrated optics a reality. Researchers at the Massachusetts Institute of Technology (MIT), supported by NSF, are addressing the multicore programming challenge by developing high-performance on-chip networks.[13] The team is investigating ways to use these devices to build energy-efficient, high-performance networks that allow hundreds (or thousands) of processing cores to work together. The Air Force Office of Scientific Research (AFOSR) Optoelectronics and Photonics program explores nanotechnology approaches to optoelectronic information processing, integrated photonics, and associated optical and photonic device components for air and space platforms to transform Air Force capabilities in computing, communications, storage, sensing, and surveillance. Major areas of emphasis are nanophotonics and nanofabrication. For example, the Integrated Hybrid Nanophotonic Circuits effort led by Stanford University (Figure 2) is an AFOSR Multidisciplinary University Research Initiative (MURI) project[14] aimed at developing electrically driven plasmon sources that, via short plasmonic waveguides, can be coupled to low-loss dielectric waveguides and plasmonic circuit elements. Such advantages are integral to developing advanced communication systems that can be utilized in military as well as other applications.

In July 2015, DOD awarded the American Institute for Manufacturing Integrated Photonics to a consortium of 124 companies, nonprofits, and universities led by the Research Foundation for the State University of New York. With a total investment of over $610 million—$110 million in Federal funds and more than $500 million in non-Federal contributions—the announcement marked the largest public-private commitment as of 2016 for a manufacturing institute launched in the United States.

[12] www.src.org/program/starnet/
[13] groups.csail.mit.edu/carbon/?page_id=62
[14] web.stanford.edu/~markb29/muri/index.html

Given the highly desirable electronic properties of some carbonaceous nanomaterials, such as their ability to conduct electricity with almost no resistance, Thrust 3 of this NSI encourages research into **nanoelectronics derived from carbon nanotubes and graphene**. The interest in using graphene as an electronic material arises from the high speed with which electrons move through the material—approximately 100 times faster than in silicon. NASA's Goddard Space Flight Center (GSFC) has developed a program in the synthesis and processing of large-area, high-quality graphene, and the development of graphene-based devices. Some of the applications that GSFC has focused on are graphene transparent electrodes, integrated graphene strain sensors for structural health monitoring of composite structures, graphene-gallium nitride ultraviolet detectors, and ultrasensitive chemical sensors. In addition, GSFC collaborators have demonstrated logic circuits and memory devices based on graphene. NIST has organized a graphene team to develop measurement and modeling techniques to understand mechanical-strain-induced interactions. The researchers have shown that straining graphene membranes induces pseudomagnetic fields that confine the graphene's electrons and create quantized quantum-dot-like energy levels. By investigating graphene's electronic band gap, the NIST team helps to address the technical aims outlined under this thrust that relates to graphene-based active devices. In addition, NIST researchers are making major advances in producing carbon-based nanomaterials for nanoelectronics. They have developed a rapid and economical method to produce high-purity samples of carbon nanotubes and techniques to monitor their purity. NSF and AFOSR have partnered on a solicitation entitled Two-Dimensional Atomic-layer Research and Engineering (2-DARE),[15] through the NSF Office of Emerging Frontiers in Research and Innovation. AFOSR program officers have collaborated with NSF in the review, selection, and potential funding of proposals submitted under this solicitation. Interest in this topic stems from the rapid and recent advances in graphene that have raised enticing questions regarding other examples of 2D materials (Figure 3) that might have distinct and useful properties, such as hexagonal boron nitride (h-BN); transition metal dichalcogenides; the chalcogenides of group III, group IV, and group V; transition metal oxides; tertiary compounds of carbo-nitrides; and other traditionally nonlayered structures such as germanene (atomic layers of germanium) and silicene (silicon-based layered structures).

The Federal Government supports a robust R&D effort on **quantum information systems**. For example, in 2012 a NIST researcher shared the Nobel Prize in Physics for ground-breaking experimental methods that enable measuring and manipulation of individual quantum systems. Although quantum information systems may have a great impact on future computer designs, the quantum information and nanotechnology communities operate more independently than envisioned in the 2010 Nanoelectronics NSI white paper. Presently, there are also numerous, independent, well-funded quantum computing programs throughout the private sector. Examples include research in superconducting loops at Google, IBM, and Quantum Circuits; research in trapped ion quantum logic at ionQ; research in silicon quantum dots at Intel; research in diamond vacancy quantum logic at Quantum Diamond Technologies;

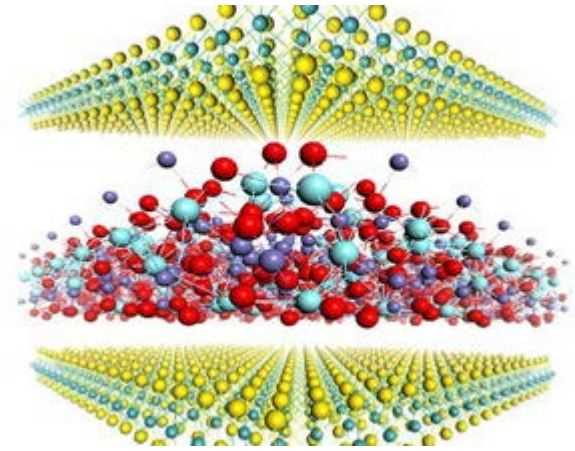

Figure 3. Illustration of a heterogeneous structure made with 2D van der Waals materials. (Source: NSF)

[15] www.nsf.gov/pubs/2015/nsf15502/nsf15502.htm?WT.mc_id=USNSF_179

and research in topological qubits at Microsoft and Bell Laboratories.[16] Among the largest single investments was Intel's $50 million investment in QuTech.

The 2010 white paper envisioned that agencies participating in the signature initiative would benefit from a university-based network of user facilities for the **fabrication and characterization of nanoelectronic materials and devices**. The National Nanotechnology Coordinated Infrastructure (NNCI)[17] network, supported by NSF, consists of 16 regional centers and is the successor to the National Nanotechnology Infrastructure Network. Since some of the nodes partner with other universities, the NNCI consists of laboratories at 24 universities, and has several college and community college education and outreach partners. The user facility sites include capabilities and instrumentation addressing current and anticipated future user needs across the broad areas of nanoscale science, engineering, and technology. NIST and the DOE also support this thrust with user facilities. NIST's Center for Nanoscale Science and Technology[18] supports the U.S. nanotechnology enterprise from discovery to production by providing industry, academia, NIST, and other government agencies with access to world-class nanoscale measurement and fabrication methods and technology. The five Nanoscale Science and Research Centers (NSRCs)[19] are DOE's premier user centers for interdisciplinary research at the nanoscale, serving as the basis for a national program that encompasses new science, tools, and computing capabilities. NSRCs are co-located or in close proximity to other DOE facilities (e.g., specialized light sources) that are also important to nanoelectronics research.

Nanoelectronics is a key enabler for the continued advancement of information technology. The Nanoelectronics for 2020 and Beyond NSI has addressed R&D gaps, leveraged skills and investments among multiple agencies, provided a forum for communication and technology assessment, and catalyzed communities of interest among agencies, industry, and academia. The agencies participating in the Nanoelectronics NSI have made considerable progress towards accomplishing the expected outcomes envisioned in this NSI since they were defined in the 2010 white paper. This document presents a broad overview of this progress by highlighting some examples of projects and accomplishments in each thrust area. These highlights illustrate the rapidly evolving nature of nanoelectronics. There are furthermore several initiatives, grand challenges, programs, and partnerships that did not exist at the inception of the Nanoelectronics NSI but now support the thrusts in major ways. The National Strategic Computing Initiative[20] and Nanotechnology-Inspired Grand Challenge for Future Computing[21] both provide frameworks for looking beyond the von Neumann architectures, creating a viable path for future computing systems after the limits of current semiconductor technology are reached ("post-Moore's Law era"). The American Institute for Manufacturing Integrated Photonics, the Flexible Hybrid Electronics Manufacturing Innovation Institute, and the Next Generation Power Electronics Institute[22] will advance nanoscale circuit, device, and materials research while simultaneously providing state-of-the-art fabrication, packaging, and testing facilities. Finally, the two 2017 programs from the SRC, JUMP and nCORE, in collaboration with DARPA and NSF's E2CDA, will address multiple emerging challenges in computing paradigms, device and materials research, manufacturing and nanofabrication, metrology and characterization, and computational modelling of materials and devices.

[16] www.sciencemag.org/news/2016/12/scientists-are-close-building-quantum-computer-can-beat-conventional-one?utm_campaign=news_daily_2016-12-01&et_rid=17050433&et_cid=1031549
[17] www.nnin.org/news-events/news/nnci-award
[18] www.nist.gov/cnst/
[19] www.science.energy.gov/bes/suf/user-facilities/nanoscale-science-research-centers/
[20] www.nitrd.gov/nsci/
[21] www.nano.gov/futurecomputing
[22] manufacturingusa.com/institutes